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J. Howard Smith

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MCDERMOTT WILL & EMERY LLP  
18191 VON KARMAN AVE.  
SUITE 500  
IRVINE, CA 92612-7108

EXAMINER

SHAH, CHIRAG G

ART UNIT

PAPER NUMBER

2664

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/780,979

Applicant(s)

SMITH ET AL.

Examiner

Chirag G. Shah

Art Unit

2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 2/21/05.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 2/9/01 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments, see Remarks, filed 6/29/05, with respect to the rejection(s) of claim(s) 1 under page 11 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Rostoker et al. (U.S. Patent No. 5,640,399).

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 5, 9, 10, 12, 14 and 16 rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (U.S. Patent No. 5,640,399), hereinafter Rostoker.

Referring to claims 1 and 16, Rostoker discloses in **fig. 32 and claim 1 of a single chip router 200** having a communication controller [**controller, fig. 32**] comprising:

a memory circuit [**RAM 206 and 208, see fig. 32**];

a processor [**RISC CPU 204, see fig. 32 and col. 65, lines 1-21**] operable in response to data and instructions stored in the memory circuit [**RAM CPU 204, see fig. 32**];

a first communication circuit [**First of the protocol interface 216 unit, see fig. 32 and claim 1**] under control of the processor [**RISC CPU 204**] for communicating between the

Art Unit: 2664

communication controller and a first remote device [device attached to 10Base T interface, see figs. 32 and 2] according to a first data communication standard [first protocol, see fig. 32 and claim 1]; and

a second communication circuit [second of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between communication controller and a second remote device [device attached to serial interface, see figs. 32 and 2] according to a second data communication standard [second protocol, see fig. 32 and claim 1], the second data communication standard being different from the first data communication standard [see col. 8, lines 7-8 and fig. 32, where different multiprotocol single chip router is disclosed],

wherein the communication controller is integrated in a single integrated circuit [the layout of components of a single chip router is fabricated on an integral substrate, see fig. 32, 36 and 37].

Referring to claims 5, Rostoker disclose based on in figs. 32, 2 and 37 where in the second communication circuit may comprise an Ethernet bus controller as claim.

Referring to claim 9, Rostoker discloses based on fig. 32, 2, and 37 of an Ethernet bus controller under control of the processor [RISC CPU Processor, see fig. 32] for communicating between the communication controller [controller, fig. 32] and a third remote device according to Ethernet data communication standard [device being communicated from Ethernet interface to as in fig. 2 and 32] as claim.

Art Unit: 2664

Referring to claim 10, Rostoker disclose in figure 32 of further comprising an asynchronous serial data communication circuit [serial interface 234; fig. 32].

Referring to claim 12, Rostoker discloses in fig. 32 and 37 of the controller further comprising an internal communication bus [system bus, see fig. 32] coupled to the processor [RISC CPU 204, fig. 32] , the first communication circuit [ first of the protocol interface 216 unit, see fig. 32 and claim 1], the second communications circuit [second of the protocol interface 216 unit, see fig. 32 and claim 1] and Ethernet bus controller standard [Ethernet interface controller, see fig. 32 and 37].

Referring to claim 14, Rostoker discloses in figure 32 of further comprising wherein the memory circuit comprises a boot read only memory (instructions RAM) and read-write memory (DATA RAM).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3-4, 6-7, 17-19, 21, 24-25, and 32 rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of Jundt et al. (U.S. Patent No. 6,618,630), hereinafter referred as Jundt.

Referring to claims 3, 4, 17 and 18, Rostoker fails to disclose wherein the first communication circuit comprises a ProfiBus or CAN circuit controller for external communication according to ProfiBus or CAN communication protocol. Jundt discloses wherein the first communication circuit comprises a ProfiBus or CAN circuit controller for external communication according to ProfiBus or CAN communication protocol [see figure 1 and column 4, lines 41 to 66, the controller 12 communicates with the field devices 18 via any desired or standard I/O cards 22, the first of the plurality of I/O card 22 may communicate with field device using PROFIBUS or CAN] as claims. Therefore, it would have been obvious to one of ordinary skills the art at the time of the invention to include the features of including a CAN bus controller format or ProfiBus as taught by Jundt. One is motivated as such in order to communicate and interoperate with devices using any desired format or protocol.

Referring to claims 6 and 7, Rostoker fails to disclose wherein the second circuit comprises the CAN bus controller having a logic circuit configured to receive and transmit data according to the CAN standard. Jundt discloses wherein the second circuit comprises the CAN bus controller having a logic circuit configured to receive and transmit data according to the CAN standard [see figure 1, column 4, lines 5-66] as claim. Therefore, it would have been obvious to one of ordinary skills the art at the time of the invention to include the features of including a CAN bus controller format as taught by Jundt. One is motivated as such in order to communicate and interoperate with devices using any desired format or protocol.

Art Unit: 2664

Referring to claim 19, Rostoker disclose in fig. 32 of wherein the processing means [RISC CPU 204, see fig 32] comprises: a processor coupled to the first communication means [First of the protocol interface 216 unit, see fig. 32 and claim 1] and the second communication means [second of the protocol interface 216 unit, see fig. 32 and claim 1].

Referring to claim 21, Rostoker discloses in fig. 32 of a single chip router including an integrated circuit comprising:

a processor block [RISC CPU processor 204, fig. 32] which controls operation of the integrated circuit;

a memory block [instruction and data RAM, see fig. 32] which stores data and instructions for use by the processor block;

a first data communication port [first port for first protocol interface unit, see fig. 32 and claim 1] ;

a second data communication port [second port for second protocol interface unit, see fig. 32 and claim 1]; and

an internal bus [system bus, see fig. 32] coupling the processor block [RISC CPU 204, fig. 32], the memory block [206 and 208, fig. 32], the first control blocks and the second control blocks.

Rostoker discloses in col. 8, lines 7-8 that the single chip router support multiprotocol. *Rostoker fails to explicitly disclose a ProfiBus control block coupled with the first data communication port and a Controller Area Network (CAN) control clock coupled with the*

Art Unit: 2664

*second data communication port; and the internal bus is respectively coupled to the respective control blocks.*

Jundt disclose a ProfiBus control block coupled with the first data communication port [any desired format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18]; a second data communication port [second of the plurality of I/O cards 22]; a Controller Area Network (CAN) control block coupled with the second data communication port [any desired format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18]; and Jundt further discloses in column 4, lines 41-45 that the controller includes memory and processor that executes the process control solution and that controller communicates with the field device via CAN or any desired standard I/O device 22. Therefore, it would have been obvious to one of ordinary skills the art at the time of the invention to include the features of coupling first and second ports with any desired control block format as taught by Jundt. One is motivated as such in order to communicate and interoperate with devices using any desired format or protocol.

Referring to claim 24, Rostoker discloses in fig. 32 and claim 1 of a single chip router 200 having a communication controller [controller, fig. 32] for controlling a number of data interfaces connected to the system bus comprising:

a memory circuit [RAM 206 and 208, see fig. 32];

a processor [RISC CPU 204, see fig. 32 and col. 65, lines 1-21] operable in response to data and instructions stored in the memory circuit [RAM CPU 204, see fig. 32];

Art Unit: 2664

a plurality of communication circuit [First and second of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between the communication controller and plurality of devices

wherein the communication controller is integrated in a single integrated circuit [the layout of components of a single chip router is fabricated on an integral substrate, see fig. 32, 36 and 37].

Rostocker fails to explicitly disclose of a ProfiBus controller comprising: a ProfiBus core; a processor; a memory for storing data and instructions for operation by the processor; at least one control circuit which controls wireline data communications according to a standard other than Profibus standard; and an internal bus for internal data communications within the ProfiBus controller, wherein the ProfiBus controller is integrated in an integrated circuit.

Jundt discloses in figure 1 of a ProfiBus controller 12 comprising:

a ProfiBus core [first of the plurality of I/O cards 22; the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18];

a processor [as disclosed in column 4, lines 41 to 45];

a memory [as disclosed in figure 1 and in column 4, lines 41 to 45];;

at least one control circuit which controls wireline data communication according to a standard other than ProfiBus standard [the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the

Art Unit: 2664

controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18 and further more control circuit controls wireline data communication to field device 18 in any desired format such as HART, PROFIBUS, WORLDVIEW, DeviceNet and CAN as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18] as claim.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of replacing the communications controller integrated into an integrated circuit of Rostocker with that of a Profibus controller as taught by Jundt. One is motivated as such in order to communicate and interoperate with devices using any desired format or protocol.

Referring to claims 25, Jundt discloses wherein the second circuit comprises the CAN bus controller having a logic circuit configured to receive and transmit data according to the CAN standard [see figure 1, column 4, lines 5-66] as claim.

Referring to claim 32, Rostoker discloses in **fig. 32 and claim 1 of a single chip router 200** having a communication controller [controller, fig. 32], fabricated on a circuit (single chip, see fig. 32), for communication between two devices (devices attached to local area network interfaces and wide area network interface, see fig. 32), comprising: a plurality of interface circuits comprising:

an Ethernet Interface circuit for communication using Ethernet communication standard [see figures 1 and 32];

Art Unit: 2664

a processor [RISC CPU 204, see fig. 32 and col. 65, lines 1-21] operable in response to data and instructions stored in the memory circuit [RAM CPU 204, see fig. 32];

a first communication circuit [First of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between the communication controller and a first remote device [device attached to 10Base T interface, see figs. 32 and 2] according to a first data communication standard [first protocol, see fig. 32 and claim 1]; and

a second communication circuit [second of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between communication controller and a second remote device [device attached to serial interface, see figs. 32 and 2] according to a second data communication standard [second protocol, see fig. 32 and claim 1], the second data communication standard being different from the first data communication standard [see col. 8, lines 7-8 and fig. 32, where different multiprotocol single chip router is disclosed],

a memory circuit [RAM 206 and 208, see fig. 32];

Rostocker fails to disclose that one of the interface circuits may be a fieldbus interface circuit for communication using a fieldbus communication standard.

Jundt discloses in figure 1 and column 3, lines 56 to column 4, lines 66 a communication controller 12, fabricated on a circuit, for communication between at least two devices (one of workstations 14 and field device 18), comprising:

a plurality of interface circuits selected from a group consisting of an Ethernet Interface circuit for communication using Ethernet communication standard; a Controller Area Network

Art Unit: 2664

interface circuit for communication using a Controller Area Network communication standard; and a field bus interface circuit for communication using a fieldbus communication standard, wherein at least two of the interface circuits are different [the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18, format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18];

a processor [as disclosed in column 4, lines 41-5] for controlling the communication between the communication controller 12 and a first device 14 using a first interface circuit [Ethernet] the plurality of interface circuits and between the communication controller 12 and a second device 18 using a second interface circuit of the plurality of interface circuits, wherein the first circuit is different from the second interface circuit [I/O cards 22 using any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN as disclosed in column 4, lines 41 to 66 using a second interface circuit of the plurality of interface circuits, wherein the first circuit [Ethernet] is different from the second interface circuit [any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN] as claim] and a processor for controlling the communication between the communication controller 12 and a first device 14 using the Ethernet interface circuit [as disclosed in column 3, lines 56 to column 4, lines 4] and between the communication controller 12 and a second device 18 using the fieldbus interface circuit [as disclosed in column 4, lines 41-66]. Therefore, it would have been

Art Unit: 2664

obvious to one of ordinary skills in the art at the time of the invention to include a fieldbus interface circuit as one of the interface devices as taught by Jundt into Rostocker's invention.

One is motivated as such in order to provide interface cards that communicate with any desired format or protocol for interoperability.

6. Claims 13, 20, 23, and 27-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of Jundt as applied to claims above, and further in view of NetSilicon (NET+12).

Referring to claim 13, Rostoker in view of Jundt fails to disclose a communication controller comprising a SPI bus controller. NetSilicon discloses of an Embedded Ethernet/Internet-Ready Processor and discloses on the NET+12 Processor Block Diagram and in the Hardware Specification section of further comprising a DMA controller having 4 dedicated channels for a Serial Peripheral Interconnect (serial transmit and receive) bus controller as claim. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Rostoker in view of Jundt to include an controller comprising an SPI bus controller as taught by NetSilicon in order to support multitude of different transmission protocols in a fully integrated solution.

Referring to claim 20, NetSilicon discloses in the NET+12 Processor Block Diagram and in the Hardware Specification of further comprising: an interface means for serial communication (2 Serial Port) with an external data source for loading at least a portion of the

Art Unit: 2664

memory (Programmable Memory Controller) means upon initialization of the data communication device.

Referring to claims 23 and 27, NetSilicon discloses in the NET+12 Processor Block Diagram of an Integral 10/100 Ethernet MAC control block coupled to the internal bus.

Referring to claim 28, NetSilicon discloses in the NET+12 Processor Block Diagram wherein the processor comprises a serial communication port (2 Serial Ports, Asynchronous and Synchronous Serial Data and Control) for external data communication as claim.

Referring to claim 29, NetSilicon discloses in the NET+12 Processor Block Diagram and in the Hardware Specification of further comprising: program code stored in a first portion of the memory (SRAM) and executable by the processor (RSIC Processor) for controlling loading of data and instructions from an external data source by the serial communication port (2 Serial Port) to a second portion of memory (ROM).

7. Claims 8, 11, 15, 22 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of Jundt as applied to claims above, and further in view of Gotze (U.S. Patent No. 5,941,966).

Referring to claims 8, 22 and 26, Rostocker in view of Jundt discloses a single chip router having circuit with a CAN bus controller. Rostocker in view of Jundt fails to disclose of a circuit having a second CAN control block. Gotze disclose a first CAN control block 510 and other

Art Unit: 2664

control block 520, which can serve as second CAN control block. Gotze discloses in figure 2 of drivers associated with the respective Bus of Figure 4 are coupled to the internal bus. Therefore, it would have been obvious to one of ordinary skills the art at the time of the invention to include the features of including a second CAN bus controller format as taught by Gotze. One is motivated as such in order to communicate and interoperate with devices using any desired format or protocol.

8. Referring to claim 11, and 15, Rostocker in view of Jundt discloses a single chip router having circuit with a CAN bus controller. Rostocker in view of Jundt fails to disclose of CAN bus controller with two or more asynchronous Gotze disclose wherein the CAN bus controller comprises two or more asynchronous serial data communication circuits [Figure 4, RS-232 515 and other 520 server as two or more asynchronous serial data communication circuits]. Therefore, it would have been obvious to one of ordinary skills the art at the time of the invention to include the features of including a CAN bus controller with two or more serial data communication circuits as taught by Gotze. One is motivated as such in order to communicate and interoperate with devices using any desired format or protocol.

9. Claims 30-31 and 33-34 rejected under 35 U.S.C. 103(a) as being unpatentable over Rostocker in view of Jundt and further in view of Net Silicon (NET+12).

Regarding claims 30-31, Rostoker discloses in **fig. 32 and claim 1 of a single chip router 200** having a communication controller [controller, fig. 32], fabricated on a circuit (single chip, see fig. 32), for communication between two devices (devices attached to local

Art Unit: 2664

**are network interfaces and wide area network interface, see fig. 32], comprising: a plurality of interface circuits comprising:**

an Ethernet Interface circuit for communication using Ethernet communication standard [see figures 1 and 32];

a processor [RISC CPU 204, see fig. 32 and col. 65, lines 1-21] operable in response to data and instructions stored in the memory circuit [RAM CPU 204, see fig. 32];

a first communication circuit [First of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between the communication controller and a first remote device [device attached to 10Base T interface, see figs. 32 and 2] according to a first data communication standard [first protocol, see fig. 32 and claim 1]; and

a second communication circuit [second of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between communication controller and a second remote device [device attached to serial interface, see figs. 32 and 2] according to a second data communication standard [second protocol, see fig. 32 and claim 1], the second data communication standard being different from the first data communication standard [see col. 8, lines 7-8 and fig. 32, where different multiprotocol single chip router is disclosed],

a memory circuit [RAM 206 and 208, see fig. 32];

Rostocker fails to disclose that one of the interface circuits may be a controller area network interface for communication using a controller area network communication standard.

Art Unit: 2664

Jundt discloses in figure 1 and column 3, lines 56 to column 4, lines 66 of a communication controller 12, fabricated on a circuit, for communication between at least two devices (one of workstations 14 and field device 18), comprising: a plurality of interface circuits comprising: a Controller Area Network interface circuit for communication using a Controller Area Network communication standard [see figure 1 and column 4, lines 41 to 66];

a processor [as disclosed in column 4, lines 41-45] for controlling the communication between the communication controller 12 and a first device 14 using a first interface circuit [Ethernet as disclosed in column 3, lines 56 to column 4, lines 4] of the plurality of interface circuits and between the communication controller 12 and a second device 18 [I/O cards 22 using any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN as disclosed in column 4, lines 41 to 66 using a second interface circuit of the plurality of interface circuits, wherein the first circuit [Ethernet] is different from the second interface circuit [any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN] as claim. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to include a CAN controller as one of the interface devices as taught by Jundt into Rostocker's invention. One is motivated as such in order to provide interface cards that communicate with any desired format or protocol for interoperability.

Rostocker in view of Jundt further fails to disclose of having a communication controller fabricated as an integrated circuit and having an option to select a Serial Peripheral Interface Circuit for communication using a SPI communication standard among the other desired formats or protocols.

NetSilicon discloses of an Embedded Ethernet/Internet-Ready Processor and discloses in paragraph 1 of the first page, the NetSilicon NET+12 is a high-performance highly integrated 32-bit microprocessor having DMA controller, Ethernet MAC controller and memory controller among a plurality of communication standards designed for use in networked devices.

NetSilicon further discloses on the NET+12 Processor Block Diagram and in the Hardware Specification section of further comprising a DMA controller having 4 dedicated channels for a Serial Peripheral Interconnect (serial transmit and receive) bus controller. NetSilicon additionally discloses in the NET+12 Processor Block Diagram of the controller having a Programmable Memory Controller block supporting ROM and SRAM having the functionality of volatile and non-volatile memory.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Rostocker in view Jundt to include the features of SPI, ROM and SRAM in the controller fabricated as an integrated circuit as taught by NetSilicon. One is motivated as such in order to ensure complete scalability and compatibility for supporting a plurality of communication standard in use today, while assuring a reliable network performance.

Referring to claims 33 and 34, Rostoker discloses in **fig. 32 and claim 1 of a single chip router 200** having a communication controller [**controller, fig. 32**], fabricated on a circuit (single chip, see fig. 32), for communication between two devices (devices attached to local are network interfaces and wide area network interface, see fig. 32), comprising: a plurality of interface circuits comprising:

Art Unit: 2664

an Ethernet Interface circuit for communication using Ethernet communication standard [see figures 1 and 32];

a processor [RISC CPU 204, see fig. 32 and col. 65, lines 1-21] operable in response to data and instructions stored in the memory circuit [RAM CPU 204, see fig. 32];

a first communication circuit [First of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between the communication controller and a first remote device [device attached to 10Base T interface, see figs. 32 and 2] according to a first data communication standard [first protocol, see fig. 32 and claim 1]; and

a second communication circuit [second of the protocol interface 216 unit, see fig. 32 and claim 1] under control of the processor [RISC CPU 204] for communicating between communication controller and a second remote device [device attached to serial interface, see figs. 32 and 2] according to a second data communication standard [second protocol, see fig. 32 and claim 1], the second data communication standard being different from the first data communication standard [see col. 8, lines 7-8 and fig. 32, where different multiprotocol single chip router is disclosed],

a memory circuit [RAM 206 and 208, see fig. 32];

Rostocker fails to disclose that one of the interface circuits may be a fieldbus interface circuit for communication using a fieldbus communication standard.

Jundt discloses in figure 1 and column 3, lines 56 to column 4, lines 66 a communication controller 12, fabricated on a circuit, for communication between at least two devices (one of workstations 14 and field device 18), comprising:

Art Unit: 2664

a plurality of interface circuits selected from a group consisting of an Ethernet Interface circuit for communication using Ethernet communication standard; a Controller Area Network interface circuit for communication using a Controller Area Network communication standard; and a field bus interface circuit for communication using a fieldbus communication standard, wherein at least two of the interface circuits are different [the controller 12 communicates with the field devices 18 via any desired or standard I/O Cards 22, the I/O cards 22 may be analog I/O cards that connect the controller 12 to the field devices 18 may be digital or combined digital and analog and analog I/O cards that communicate using any desired format or protocols as disclosed in column 4, lines 41 to column 5, lines 18, format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN; as disclosed in figure 1, claim 1, and column 4, lines 5 to column 5, lines 18];

a processor [as disclosed in column 4, lines 41-5] for controlling the communication between the communication controller 12 and a first device 14 using a first interface circuit [Ethernet] the plurality of interface circuits and between the communication controller 12 and a second device 18 using a second interface circuit of the plurality of interface circuits, wherein the first circuit is different from the second interface circuit [I/O cards 22 using any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN as disclosed in column 4, lines 41 to 66 using a second interface circuit of the plurality of interface circuits, wherein the first circuit [Ethernet] is different from the second interface circuit [any desired protocol or format such as HART, PROFIBUS, WORLDFIP, DeviceNet and CAN] as claim] and

a processor for controlling the communication between the communication controller 12 and a first device 14 using the Ethernet interface circuit [as disclosed in column 3, lines 56 to

Art Unit: 2664

column 4, lines 4] and between the communication controller 12 and a second device 18 using the fieldbus interface circuit [as disclosed in column 4, lines 41-66]. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to include a fieldbus interface circuit as one of the interface devices as taught by Jundt into Rostocker's invention. One is motivated as such in order to provide interface cards that communicate with any desired format or protocol for interoperability. Rostocker in view of Jundt further fails to disclose of having a communication controller fabricated as an integrated circuit and having an option to select a Serial Peripheral Interface Circuit for communication using a SPI communication standard among the other desired formats or protocols.

NetSilicon discloses of an Embedded Ethernet/Internet-Ready Processor and discloses in paragraph 1 of the first page, the NetSilicon NET+12 is a high-performance highly integrated 32-bit microprocessor having DMA controller, Ethernet MAC controller and memory controller among a plurality of communication standards designed for use in networked devices. NetSilicon further discloses on the NET+12 Processor Block Diagram and in the Hardware Specification section of further comprising a DMA controller having 4 dedicated channels for a Serial Peripheral Interconnect (serial transmit and receive) bus controller. NetSilicon additionally discloses in the NET+12 Processor Block Diagram of the controller having a Programmable Memory Controller block supporting ROM and SRAM having the functionality of volatile and non-volatile memory.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Rostocker in view of Jundt to include the features of SPI, ROM and SRAM in the controller fabricated as an integrated circuit as taught by

Art Unit: 2664

NetSilicion. One is motivated as such in order to ensure complete scalability and compatibility for supporting a plurality of communication standard in use today, while assuring a reliable network performance.

***Conclusion***

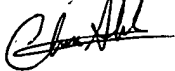
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7682. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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cgs

March 10, 2006



Chirag Shah  
Patent Examiner, Division 2616